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EXAMINER
BECK, ALEXANDER S

ART UNIT	PAPER NUMBER
2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/500,237	TAMURA ET AL.	
	Examiner	Art Unit	
	ALEXANDER S. BECK	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 April 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-7,9-13 and 15-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-7,9-13 and 15-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *04 May 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *20090311*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

RESPONSE TO AMENDMENT

1. Acknowledgment is made of the amendment filed Apr. 8, 2009 ("Amend."), in which the rejections of the claims are traversed. Claims 1, 3-7, 9-13 and 15-22 are currently pending and an Office action on the merits follows.

INFORMATION DISCLOSURE STATEMENT

2. The information disclosure statement filed Mar. 11, 2009, has been acknowledged and considered by the examiner. An initialed copy of the PTO-1449 is included in this correspondence.

CLAIM REJECTIONS - 35 USC § 103

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

4. Claims 1, 3-7, 9, 13, 15, 16 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,765,551 to Nakano et al. ("Nakano") in view of U.S. Patent No. 7,042,427 to Inukai ("Inukai").

As to claim 1, Nakano discloses an image display device (Nakano, 80), comprising:

a circuit (Nakano, 10) for generating drive signals from an input image signal;

a plurality of pixels including a light emitting element for emitting light of a predetermined color of red, green or blue by being applied with said drive signal supplied for each color from said circuit;

an adjustment information retrieve means (Nakano, 40, 50) for obtaining information relating to light emission adjustment proportional to a change in color balance of said light emitting elements (Nakano, col. 3, ll. 4-11 and 29-32; see also col. 9, ll. 11-15);

a level adjustment circuit (Nakano, 70) provided in said circuit for changing a level of an RGB signal before divided to said drive signals for respective RGB colors based on said information obtained by said adjustment information retrieve means (Nakano, col. 6, ll. 36-40; see also col. 8, ll. 51-54); and

wherein said level adjustment circuit changes a level of a direct current voltage supplied to said circuit, proportionally to account for the changing color balance of the change in luminance of said light emitting element (Nakano, Figs. 1 and 8).

It is noted that although a liquid crystal display device is illustrated in the above example, Nakano discloses wherein a wide range of matrix-type image display devices may be used, such as an electroluminescent (EL) display device (Nakano, col. 8, ll. 31-35).

Nakano does not disclose expressly wherein:

(1) said adjustment information retrieve means obtains information relating to light emission adjustment proportional to the deterioration of said light emitting element; and

(2) said adjustment information retrieve means and said level adjustment circuit further comprise (a) a plurality of pixels, including pixels of at least each respective RGB color and (b) a detection means for detecting a change value corresponding to the

luminance of the plurality of pixels by measuring the voltage between the ends of the light emitting elements.

Inukai discloses a method of maintaining color balance in an EL display, analogous to that of Nakano (Inukai, col. 7, ll. 19-29). Furthermore, Nakano discloses means for obtaining information relating to light emission adjustment proportional to the deterioration of red green and blue light emitting elements and detection means for detecting a change value corresponding to the luminance of the plurality of pixels by measuring the voltage (i.e., current) between the ends of the light emitting elements (Inukai, Abstract; see also col. 7, ll. 19-29).

At the time the invention was made, it would have been obvious to one having ordinary skill in the art to modify the image display device of Inukai such that the display further comprised detection means for obtaining information relating to light emission adjustment proportional to the deterioration of the light emitting element and changing color balance of the display, as taught by Inukai, such that the information was used to change a level of an RGB signal before dividing said drive signals to respective RGB colors based on said information obtained for preventing a changing color balance, as taught by Nakano. The suggestion/motivation for doing so would have been to suppress an unwanted changing color balance in a RGB image display device.

As to claim 13, Nakano discloses a color balance adjustment method of an image display device (Nakano, 80), comprising a plurality of pixels including a light emitting element for emitting light of a predetermined color of red, green or blue in accordance with an input drive signal, including:

a step of obtaining information relating to light emission adjustment of said light emission element (Nakano, elements 40 and 50; see also col. 3, ll. 4-11 and 29-32; col. 9, ll. 11-15);

a step of changing a level of an RGB signal before dividing said RGB signal into said drive signals of respective RGB colors based on said information on light emission adjustment (Nakano, element 70; see also col. 6, ll. 36-40; col. 8, ll. 51-54); and

a step of generating said drive signals by dividing said RGB signal into the respective colors time-series pixel data and supplying to said pixels corresponding thereto; and

wherein in the step of changing a level of said RGB signal, a level of the direct current voltage is supplied to a circuit for performing signal processing on an image signal and generating said drive signals, proportionally to the change in luminance of said light emitting element (Nakano, Figs. 1 and 8).

It is noted that although a liquid crystal display device is illustrated in the above example, Nakano discloses wherein a wide range of matrix-type image display devices may be used, such as an electroluminescent (EL) display device (Nakano, col. 8, ll. 31-35).

Nakano does not disclose expressly wherein the obtaining information step and said changing step include detecting a changing value corresponding to the luminance of the plurality of pixels by measuring the voltage between the ends of the light emitting elements. However, Nakano is modified by Inukai in the same manner and for the same reasons set forth in the rejection of claim 1 above. Thus, examiner respectfully submits that Nakano and Inukai taken collectively read on the claimed limitations.

As to claim 3, Nakano discloses a D/A converter (Nakano, 50) for performing digital-analog conversion on said RGB signal; wherein said adjustment information retrieve means (Nakano, 40, 50) retrieves said information relating to changes over time for each of RGB colors (e.g., changing digital values); and said level adjustment circuit (Nakano, 70) changes a reference voltage to be supplied to said D/A converter based on

said information of respective RGB colors obtained by said adjustment information retrieve means (Nakano, Fig. 8).

As to claims 4 and 15, Nakano discloses a plurality of data lines for connecting by each color said plurality of pixels repeatedly arranged by a predetermined color arrangement; and a data holding circuit (Nakano, 60) for holding the respective RGB colors time-series pixel data composing said RGB signal and outputting the pixel data held for the respective colors as said drive signals in parallel with corresponding plurality of said data lines; wherein said level adjustment circuit (Nakano, 70) adjusts a level of said drive signal of at least one color by changing a level of said direct current voltage for necessary times based on said information obtained from said adjustment information retrieve means (Nakano, 40, 50) at a timing that pixel data of a different color is input to said data holding circuit (Nakano, Fig. 8).

As to claim 5, Nakano discloses wherein a control signal input to said level adjustment circuit (e.g., 70 and digital/analog conversion switches) for changing a level of said direct current voltage is in common with a sample hold signal for controlling said data holding circuit (Nakano, 60) (e.g., implicitly suggested for the purposes of avoiding an overflow/underflow of data at the output circuit 60) (Nakano, Fig. 8).

As to claim 6, Nakano discloses wherein a control signal input to said level adjustment circuit (e.g., 70 and digital/analog conversion switches) for changing said direct current voltage is a signal in synchronization with a sample hold signal for controlling said data holding circuit (60) (e.g., implicitly suggested for the purposes of avoiding an overflow/underflow of data at the output circuit 60) (Nakano, Fig. 8).

As to claims 7 and 16, Nakano discloses wherein said adjustment information retrieve means and said level adjustment circuit comprises a memory means for storing correspondence of said changing value and a level adjustment amount of said RGB signal (e.g., implicitly suggested for selecting a predetermined reference voltage level in accordance with the gray scale level of a 6-bit data signal for each color of RGB) (Nakano, Fig. 8).

As to claims 9 and 18, note the discussion of Nakano above with respect to claims 1 and 13. Nakano discloses wherein said light emitting element is an electroluminescence light emitting element (EL) (Nakano, col. 8, ll. 31-35). Nakano does not disclose expressly wherein the light emitting element is an organic EL. However, the examiner takes Official Notice that the use of organic ELs as light emitting elements in a matrix-type image display device is old and well known in the art (e.g., see Inukai). Because ELs or organic ELs can be used in a matrix-type image display device, it would have been obvious to one skilled in the art to substitute one type of light emitting element for the other to achieve the predictable result of selectively displaying display data by controlling the brightness of the light emitting elements.

5. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Nakano and Inukai as applied to claims 1, 3-7, 9, 13, 15, 16 and 18 above, and further in view of U.S. Patent No. 6,774,578 to Tanada ("Tanada").

As to claim 17, neither Nakano nor Inukai disclose expressly wherein the step of retrieving information relating to said light emission adjustment includes a step of counting an accumulated light emission time of the pixels; and a step of determining a level adjustment amount of said RGB signal from the current accumulated light emission

time of the pixels based on the correspondence of said accumulated light emission time and the level adjustment amount of said RGB signal obtained in advance.

Tanada discloses an image display device in Figure 18 comprising a step of retrieving information relating to light emission adjustment including a step of counting an accumulated light emission time of the pixels; and a memory means for storing correspondence of said accumulated light emission time and a level adjustment value of a video signal (Tanada, col. 4, l. 54 – col. 5, l. 4).

At the time the invention was made, it would have been obvious to person of ordinary skill in the art to further modify the teachings of Nakano and Inukai such that the adjustment information retrieve means and said level adjustment circuit comprise a clocking means for counting an accumulated light emission time of the pixels and a memory means for storing correspondence of said accumulated light emission time and a level adjustment value of a video signal, as taught/suggested by Tanada, wherein the video signal is an RGB video signal, as previously discussed by Nakano. The suggestion/motivation for doing so would have been to correct degradation of an image display device. (Tanada, col. 4, l. 54 – col. 5, l. 4).

6. Claims 10-12 and 19-22 rejected under 35 U.S.C. 103(a) as being unpatentable over Nakano in view of U.S. Patent No. 6,982,686 to Miyachi et al. ("Miyachi").

As to claims 10 and 19, Nakano discloses an image display device (Nakano, 80), comprising: a circuit (Nakano, 10) for generating drive signals from an input image signal; and a plurality of pixels including a light emitting element for emitting light of a predetermined color of red, green or blue by being applied with said drive signal supplied for each color from said circuit; and wherein said circuit comprises a level adjustment circuit (Nakano, 70) for changing a level of an RGB signal before divided the RGB signal is divided to said drive signals for the respective RGB colors (Nakano, Figs. 1 and 8.) It

is noted that although a liquid crystal display device is illustrated in the above example, Nakano discloses wherein a wide range of matrix-type image display devices may be used, such as an electroluminescent (EL) display device (Nakano, col. 8, ll. 31-35).

Nakano does not disclose expressly wherein said circuit comprises a motion detection circuit for detecting motions by said image signal; wherein said level adjustment circuit changes a level of an RGB signal based on a result of the motion detection obtained from said motion detection circuit; and wherein said circuit comprises a duty ratio adjustment circuit for changing the duty ratio of a light emission time of said pixels based on the motion detection result.

Miyachi discloses a liquid crystal display comprising: a motion detection circuit for detecting motions of an image signal; a level adjustment circuit for changing a luminance level of EL elements based on a result of the motion detection obtained from the motion detection circuit; and a duty ratio adjustment circuit for changing the duty ratio of the light emission time of the EL elements based on the motion detection result (Miyachi, Figs. 37-41; see also col. 43, l. 67 – col. 44, l. 9; col. 45, ll. 50-53).

All of the component parts are known in Nakano and Miyachi. The only difference is the combination of the "old elements" into a single device by incorporating them into a single image display device. Thus, it would have been obvious to one having ordinary skill to include the motion detection means and duty ratio adjustment means taught by Miyachi into the EL display device taught by Nakano, since the operation of the motion detection means and duty ratio adjustment means are in no way dependent on the operation of the other elements of the liquid crystal display device, and motion detection means with duty ratio adjustment means could be used in combination with an EL display device to achieve the predictable results of improved display quality.

Neither Nakano nor Miyachi disclose expressly wherein the plurality of pixels each comprise a light emission control circuit whereby once the pixel receives a drive

signal, the light emitting element continues to draw on a voltage source so long as the light emission control circuit receives a signal from the duty ratio adjustment circuit.

However, the examiner takes Official Notice that the use of transistors (i.e., light emission control circuit) as switches in a pixel to control how long a light emitting element continues to draw on a voltage source is old and well-known in the art. Furthermore, examiner respectfully submits that it would have been within the purview of one having ordinary skill in the art to modify the references such that the transistor, for controlling how long a light emitting element continues to draw on a voltage source, received a signal from the duty ration adjustment circuit. Examiner respectfully submits that such a modification would have been obvious because it is old and well-known in the art that a transistor in a pixel can control how long a light emitting element continues to draw on a voltage source for illumination, and the disclosure of Miyachi suggests that the duty ratio adjustment circuit is concerned with controlling the duration of light emission for the light emitting element. Thus, the effect of the duty ratio adjustment circuit in Miyachi may be realized in an active matrix EL display device through the implementation of transistors in each pixel, as one of ordinary skill in the art would appreciate.

As to claims 11 and 20, Nakano as modified by Miyachi discloses wherein said level adjustment circuit (Nakano, 70) changes a level of a direct current voltage supplied from a circuit block in said circuit and proportional to luminance of said light emitting element (Nakano, Fig. 1).

As to claims 12 and 22, Nakano as modified by Miyachi discloses wherein said light emitting element is an electroluminescence light emitting element (EL) (Nakano, col. 8, ll. 31-35). Nakano does not disclose expressly wherein the light emitting element is an organic EL. However, the examiner takes Official Notice that the use of organic

ELs as light emitting elements in a matrix-type image display device is old and well known in the art. Because ELs or organic ELs can be used in a matrix-type image display device, it would have been obvious to one skilled in the art to substitute one type of light emitting element for the other to achieve the predictable result of selectively displaying display data by controlling the brightness of the light emitting elements.

As to claim 21, Nakano as modified by Miyachi discloses a holding step for holding for the respective RGB colors time-series pixel data composing said RGB signal when generating said driving signals; wherein, in the step of changing a level of said RGB signal, by changing the level of said direct current voltage for necessary times based on information obtained from said adjustment information retrieve means at a timing where pixel data of a different color is input to said holding step, a level of said drive signal of at least one color is adjusted (Nakano, Fig. 1).

RESPONSE TO ARGUMENTS

7. Applicant's arguments filed Apr. 8, 2009, have been fully considered but they are not persuasive.

8. Applicant argues neither Nakano nor Inukai, either alone or in combination, teach or suggest "*a level adjustment circuit provided in said circuit, for changing a level of an RGB signal* ***before*** ***dividing said drive signals to respective RGB colors*** *based on said information obtained by said adjustment information retrieve means*" (Amend., pp. 10-12).

Examiner respectfully disagrees, and submits that the claimed "*drive signals to respective RGB colors*" are taught by the analog driving voltages supplied to the data lines in Nakano that have their level changed (Nakano, col. 6, ll. 37-41) and the claimed "*RGB signal*" is taught by the RGB signal in Nakano prior to having its level changed.

Thus, examiner respectfully submits that Nakano is a fair teaching of changing a level of an RGB signal before dividing the drive signals to respective RGB colors, as claimed, because the level of the RGB signal is changed **before the analog driving voltages are divided amongst the data lines in the display**. Moreover, examiner respectfully submits that the claims as presented are absent any language that would preclude such an interpretation.

9. Applicant argues that claim 13 differentiates over the prior art of record for the same reasons discussed with respect to claim 1 (Amend., p. 12). Examiner respectfully disagrees for the same reasons presented in paragraph 8 above.

10. Applicant argues neither Miyachi nor Tanaka teach or suggest "*a level adjustment circuit for changing a level of an RGB signal before divided to said drive signals for the respective RGB colors based on a result of the motion detection obtained from said motion detection circuit*," as recited in claim 10, nor do Miyachi nor Tanaka provide a basis to modify Nakano nor Inukai to include this feature (Amend., pp. 12-14).

However, examiner respectfully submits that Nakano discloses "*a level adjustment circuit for changing a level of an RGB signal before divided to said drive signals for the respective RGB colors*," as detailed in paragraph 8 above. Furthermore, Miyachi discloses a liquid crystal display comprising: a motion detection circuit for detecting motions of an image signal; a level adjustment circuit for changing a luminance level of EL elements based on a result of the motion detection obtained from the motion detection circuit; and a duty ratio adjustment circuit for changing the duty ratio of the light emission time of the EL elements based on the motion detection result (Miyachi, Figs. 37-41; see also col. 43, l. 67 – col. 44, l. 9; col. 45, ll. 50-53).

All of the component parts are known in Nakano and Miyachi. The only difference is the combination of the "old elements" into a single device by incorporating them into a

single image display device. Thus, it would have been obvious to one having ordinary skill to include the motion detection means and duty ratio adjustment means taught by Miyachi into the EL display device taught by Nakano, since the operation of the motion detection means and duty ratio adjustment means are in no way dependent on the operation of the other elements of the liquid crystal display device, and motion detection means with duty ratio adjustment means could be used in combination with an EL display device to achieve the predictable results of improved display quality.

Neither Nakano nor Miyachi disclose expressly wherein the plurality of pixels each comprise a light emission control circuit whereby once the pixel receives a drive signal, the light emitting element continues to draw on a voltage source so long as the light emission control circuit receives a signal from the duty ratio adjustment circuit.

However, the examiner takes Official Notice that the use of transistors (i.e., light emission control circuit) as switches in a pixel to control how long a light emitting element continues to draw on a voltage source is old and well-known in the art. Furthermore, examiner respectfully submits that it would have been within the purview of one having ordinary skill in the art to modify the references such that the transistor, for controlling how long a light emitting element continues to draw on a voltage source, received a signal from the duty ration adjustment circuit. Examiner respectfully submits that such a modification would have been obvious because it is old and well-known in the art that a transistor in a pixel can control how long a light emitting element continues to draw on a voltage source for illumination, and the disclosure of Miyachi suggests that the duty ratio adjustment circuit is concerned with controlling the duration of light emission for the light emitting element. Thus, the effect of the duty ratio adjustment circuit in Miyachi may be realized in an active matrix EL display device through the implementation of transistors in each pixel, as one of ordinary skill in the art would appreciate.

11. Applicant argues that claim 19 differentiates over the prior art of record for the same reasons discussed with respect to claim 10 (Amend., p. 14). Examiner respectfully disagrees for the same reasons presented in paragraph 10 above.

CONCLUSION

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ALEXANDER S. BECK whose telephone number is (571)272-7765. The examiner can normally be reached on M-F, 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Dated: June 29, 2009

/Alexander S. Beck/
Examiner, Art Unit 2629